WHAT IS CLAIMED IS:

1. Charge-trapping memory device comprising:

a semiconductor body or substrate with at least one memory cell arranged in said semiconductor body or substrate;

source and drain regions formed by doped regions in said semiconductor body or substrate and limited by junctions;

a gate dielectric on a surface of said semiconductor body or substrate between said source and drain regions and having a layer thickness;

a gate electrode on said gate dielectric; and

a charge-trapping layer formed within said gate dielectric,

the charge-trapping layer comprising two strips which are each located between an upper boundary of said junctions and said gate-electrode and which are enclosed by said gate dielectric,

said strips being formed of a material with higher relative permittivity than the gate dielectric, and

said strips having a layer thickness which is provided relative to said layer thickness of said gate dielectric in an area between said strips and a total layer thickness of said gate dielectric in an area of said strips in such a manner that a positive voltage applied to said gate electrode and provided for inducing a Fowler-Nordheim-tunnelling of electrons into said charge-trapping layer generates an electric field strength in said area of said strips, which is larger or equal to an electric field strength in said area between said strips during a process of erasure of said memory cell.

2. Charge-trapping memory device according to claim 1, in which said gate dielectric is silicon dioxide and said charge-trapping layer is silicon nitride; and

the ratio of said layer thickness of said charge-trapping layer and said layer thickness of said gate dielectric in said area between said strips is between 0.3 and 0.7.

3. Charge-trapping memory device according to claim 1, in which said gate dielectric is silicon dioxide and said charge-trapping layer is Al_2O_3; and the ratio of said layer thickness of said charge-trapping layer and said layer thickness of said gate dielectric in said area between said strips is between 0.25 and 0.6.

4. Charge-trapping memory device according to claim 1, in which said gate dielectric is silicon dioxide and said charge-trapping layer is HfO_2; and the ratio of said layer thickness of said charge-trapping layer and said layer thickness of said gate dielectric in said area between said strips is between 0.2 and 0.5.

5. Charge-trapping memory device according to claim 1, in which said total layer thickness of said gate dielectric in said area of said strips is larger than said layer thickness of said gate dielectric in said area between said strips.

6. Charge-trapping memory device according to claim 5, in which said gate dielectric is silicon dioxide and said charge-trapping layer is silicon nitride; and

the ratio of said layer thickness of said charge-trapping layer and said layer thickness of said gate dielectric in said area between said strips is between 0.3 and 0.7.

7. Charge-trapping memory device according to claim 5, in which said gate dielectric is silicon dioxide and said charge-trapping layer is Al_2O_3; and the ratio of said layer thickness of said charge-trapping layer and said layer thickness of said gate dielectric in said area between said strips is between 0.25 and 0.6.

8. Charge-trapping memory device according to claim 5, in which said gate dielectric is silicon dioxide and said charge-trapping layer is HfO_2; and the ratio of said layer thickness of said charge-trapping layer and said layer thickness of said gate dielectric in said area between said strips is between 0.2 and 0.5.

9. A memory device comprising:

a semiconductor body or substrate with at least one memory cell arranged in said semiconductor body or substrate;

source and drain regions formed by doped regions in said semiconductor body or substrate and limited by junctions;

a gate dielectric on a surface of said semiconductor body or substrate between said source and drain regions and having a layer thickness;

a gate electrode on said gate dielectric; and

a charge-trapping layer formed within said gate dielectric,

the charge-trapping layer comprising two strips which are each located between an upper boundary of said junctions and said gate-electrode and which are enclosed by said gate dielectric,

said strips being formed of a material with higher relative permittivity than the gate dielectric, and

said strips having a layer thickness which is provided relative to said layer thickness of

said gate dielectric in an area between said strips and a total layer thickness of said gate dielectric in an area of said strips in such a manner that a positive voltage applied to said gate electrode and provided for inducing a Fowler-Nordheim-tunnelling of electrons into said charge-trapping layer generates an electric field strength in said area of said strips, which is larger or equal to an electric field strength in said area between said strips during a process of erasure of said memory cell;

wherein said memory cell is erased by applying a positive voltage to said gate electrode to induce Fowler-Nordheim-tunnelling of electrons into said charge-trapping layer;

said memory cell is programmed at one of said strips of said charge-trapping layer individually by hot hole injection effected by a negative voltage applied to said gate electrode and a positive voltage applied to one of said source and drain regions adjacent to said strip; and

said memory cell is read by applying a voltage between said source and drain regions of said memory cell, which is reverse to a voltage applied for programming.

10. The memory device according to claim 9, whereby,

in an array of memory cells comprising:

at least a first memory cell and a second memory cell adjacent to said first memory cell; and

a continuous doped region comprising as integral parts thereof a first one of said source and drain regions of said first memory cell and a first one of said source and drain regions of said second memory cell;

said first memory cell is programmed at one of said strips of said first memory cell adjacent to said first one of said source and drain regions of said first memory cell, by applying a

positive inhibit voltage to a second one of said source and drain regions of said second memory cell.

11. Method for manufacturing a memory device comprising:

a semiconductor body or substrate with at least one memory cell arranged in said semiconductor body or substrate;

source and drain regions formed by doped regions in said semiconductor body or substrate and limited by junctions;

a gate dielectric on a surface of said semiconductor body or substrate between said source and drain regions and having a layer thickness;

a gate electrode on said gate dielectric; and

a charge-trapping layer formed within said gate dielectric,

the charge-trapping layer comprising two strips which are each located between an upper boundary of said junctions and said gate-electrode and which are enclosed by said gate dielectric,

in which

in a first step, a layer of a material provided as gate dielectric and a layer of a material provided for said gate electrode are deposited and structured on said surface of said semiconductor body or substrate to form said gate electrode with sidewalls;

in a second step, an etching process is performed to remove parts of said gate dielectric from beneath said gate electrode on opposite sides of said gate electrode;

in a third step, oxide layers are produced on upper and lower surfaces, where said gate dielectric has been removed, leaving spaces provided for said strips of said charge-trapping layer;

in a fourth step, a material provided for said charge-trapping layer is deposited to fill said

spaces;

in a fifth step, excess deposits of said material are removed to form said strips;

in a sixth step, sidewall spacers are formed at said gate electrode; and

in a seventh step, an implantation is performed to produce said source and drain regions.

12. Method according to claim 11, in which

in the first step, the gate electrode is formed of polysilicon on a silicon substrate, and

in the third step, said oxide layers are produced by thermal oxidation of silicon.

13. Method according to claim 12, in which

in the third step, said oxide layers are produced so that the oxide layer on lower surfaces of said gate electrode is at least 0.5 nm thicker than the oxide layer on upper surfaces of said substrate.

14. Method according to claim 11, in which

in the first step, said gate electrode is structured so as to form part of one of a number of wordlines within an array of memory cells and

after the seventh step, an electrically conductive material is filled into interspaces between said wordlines and structured to form local interconnects, and bitlines are arranged above said local interconnects and electrically insulated from said wordlines,

said local interconnects being provided as electric connections between said source and drain regions and said bitlines,

said bitlines being contact-connected to said local interconnects in next but one of said interspaces between said wordlines, in each case to contact said source and drain regions of two of said memory cells that are subsequently arranged along said wordlines.